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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,096	04/13/2004	Kei MURAYAMA	040169	3095
23850	7590	06/29/2006	EXAMINER	
ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP 1725 K STREET, NW SUITE 1000 WASHINGTON, DC 20006			IM, JUNGHWA M	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

21

Office Action Summary	Application No.	Applicant(s)	
	10/709,096	MURAYAMA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 8 and 10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: in claim 1, line 8, “via ports” should be --via posts-- ; and in line 10, “pumps” should be --bumps--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites a unclear limitation of “ ... a via hole into which a via post is, filled is arranged in a portion in the insulating film under the connection ...” Note that the instant invention shows that a via post is formed by filling the via hole. The instant invention does not disclose that the via post is filled into the via hole. Claim 1 further recites a limitation of “ ... the electronic parts whose bump is ultrasonic flip-chip packaged to the connection pad; wherein said via posts in said via holes are positioned at positions corresponding to said bumps of said electronic parts respectively, so that said via ports function as struts which can prevent that said connection pads eat into the insulating film by withstanding pressure or ultrasonic vibration, in case that electronic parts whose pumps are ultrasonic flip-chip packaged to said connection pads...” It is confusing. Note that claim 1 recites “the electronic parts whose bump is ultrasonic

Art Unit: 2811

flip-chip packaged to the connection pad” followed by “in case that electronic parts whose pumps are ultrasonic flip-chip packaged to said connection pads.” It is also noted that the strut does not prevent the connection pad from being pressed into the insulating layer by withstanding pressure or ultrasonic vibration. Claim 2 recites the similar limitations to the ones in claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 6326561), hereinafter Watanabe in view of Kajiwara et al. (US 6798072), hereinafter Kajiwara.

Regarding claim 1, insofar as understood, Fig. 10 of Watanabe shows an electronic parts packaging structure comprising:

a wiring substrate [22, 24] in which has a structure in which a wiring pattern [4 in Fig. 1] including a connection pad to which a bump [16] of an electronic parts is bonded is provided on an insulating film, and the wiring substrate in which a via hole into which a via post is filled is arranged in a portion in the insulating film under the connection pad: wherein said via posts in said via holes are positioned at positions corresponding to said bumps of said electronic parts respectively, so that said via ports function as struts which can prevent that said connection pads eat into the insulating film by withstanding pressure.

Fig. 10 of Watanabe shows most aspect of the instant invention except that bump is ultrasonic flip-chip packaged to the connection pad. Kajiwara discloses a flip chip bonding by using ultrasonic vibration (col. 2, lines 44-60).

It would have been obvious to one of ordinary skill in the art at the time of the invention made to incorporate the teachings of Kajiwara into the device of Watanabe in order to have a flip chip bonding by using ultrasonic vibration to improve the joint connection.

Regarding claim 2, insofar as understood, Fig. 10 of Watanabe shows an electronic parts packaging structure comprising:

a wiring substrate [22, 24] which has a structure in which a wiring pattern [4 in Fig. 1] including a connection pad to which a bump [16] of an electronic parts is bonded is provided on an insulating film, and the wiring substrate in which a via hole into which a via post is filled is arranged in a predetermined portion in the insulating film.

Fig. 10 of Watanabe shows most aspect of the instant invention except that bump is ultrasonic flip-chip packaged to the connection pad and a via post is arranged in a predetermined portion of the insulating film under the wiring pattern connected to the connection pad within 200 um from the connection pad. Kajiwara discloses a flip chip bonding by using ultrasonic vibration (col. 2, lines 44-60).

It would have been obvious to one of ordinary skill in the art at the time of the invention made to incorporate the teachings of Kajiwara into the device of Watanabe in order to have a flip chip bonding by using ultrasonic vibration to improve the joint connection.

The combined teachings of Watanabe and Kajiwara fail to show that a via is arranged in a predetermined portion of the insulating film under the wiring pattern

Art Unit: 2811

connected to the connection pad within 200 um from the connection pad. However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a via post arranged in a predetermined portion of the insulating film under the wiring pattern connected to the connection pad within 200 um from the connection pad for compact package, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 8, Fig. 10 of Watanabe shows that the insulating film on the wiring substrate is made of resin (col. 9, lines 41-44).

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara as applied to claim 1 or 3 above, and further in view of Umematsu et al. (US 6399897), hereinafter Umematsu.

Regarding claim 3, the combined teachings of Watanabe and Kajiwara show most aspect of the instant invention except “the via hole is a dummy via hole and a normal via hole is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad.” Fig. 5B of Umematsu shows a semiconductor package with a wiring substrate [49] wherein the via hole is a dummy via hole [58a] and a normal via hole[58] is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad [60].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Umematsu into the device of Watanabe and Kajiwara

Art Unit: 2811

in order to have the via hole to be a dummy via hole and a normal via hole arranged separately under a predetermined portion of the wiring pattern connected to the connection pad to alleviate a cracking with a dummy via and to have a signal connection with a normal via.

Regarding claim 5, the combined teachings of Watanabe, Kajiwara and Umematsu show most aspect of the instant invention except “the normal via hole is arranged in a position that is away from the connection pad in excess of 200 um.” However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a normal via hole arranged in a position that is away from the connection pad in excess of 200 um for compact package, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller*, 105 USPQ 233.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara as applied to claim 1 above, and further in view of Ohuchi (US 6590287).

Regarding claim 10, the combined teachings of Watanabe and Kajiwara show most aspect of the instant invention except “the bump of the electronic parts is made of gold, and at least a surface layer portion of the connection pad of the wiring substrate is made of gold.”

Fig. 5 of Ohuchi shows a semiconductor package wherein the bump [5] of the electronic parts is made of gold, and at least a surface layer portion of the connection pad [7] of the wiring substrate [1] is made of gold (col. 5, lines 41-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Ohuchi into the device of Watanabe and Kajiwara in order to have the bump of the electronic parts made of gold, and at least a surface layer portion of the connection pad of the wiring substrate made of gold for easier soldering.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe and Kajiwara as applied to claim 1 above, and further in view of Umematsu and Minagawa et al. (JP-2002009444), hereinafter Minagawa.

Regarding claim 4, the combined teachings of Watanabe and Kajiwara show most aspect of the instant invention except “a plurality of via holes associated with said plurality of connection pads are arranged in a state that a dummy via hole and normal via holes are arranged mixedly, and a normal via hole is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad, in the wiring pattern in which the dummy via hole is arranged under the connection pad or the wiring pattern.”

Fig. 5B of Umematsu shows a semiconductor package with a wiring substrate [49] wherein the via hole is a dummy via hole [58a] and a normal via hole[58] is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad [60].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Umematsu into the device of Watanabe and Kajiwara in order to have the via hole to be a dummy via hole and a normal via hole arranged separately under a predetermined portion of the wiring pattern connected to the connection

Art Unit: 2811

pad to alleviate a cracking with a dummy via and to have a signal connection with a normal via.

The combined teachings of Watanabe, Kajiwara and Umematsu fail to show that “a plurality of via holes associated with said plurality of connection pads are arranged in a state that a dummy via hole and normal via holes are arranged mixedly.” Fig. 1 of Minagawa shows a wiring substrate wherein a plurality of via holes [4, 7] associated with said plurality of connection pads are arranged in a state that a dummy via hole [7] and normal via holes [4] are arranged mixedly.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Minagawa into the device of Watanabe, Kajiwara and Umematsu in order to have a dummy via hole and normal via holes arranged mixedly to withstand the pressure from the pad with a dummy via while conducting a signal with a normal via from the same pad.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2811

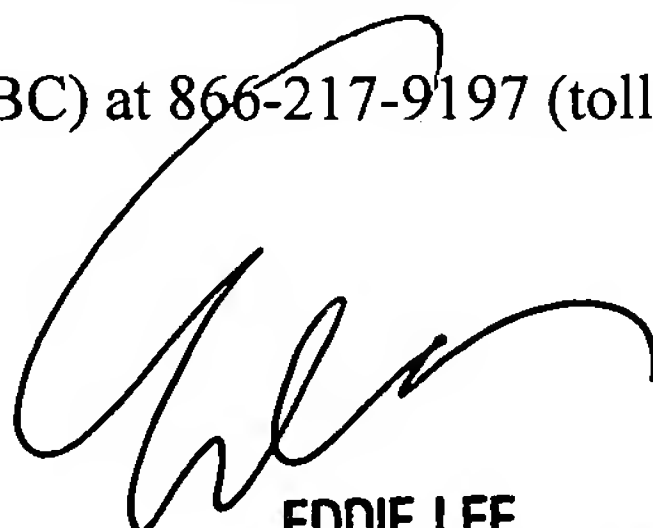
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi



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